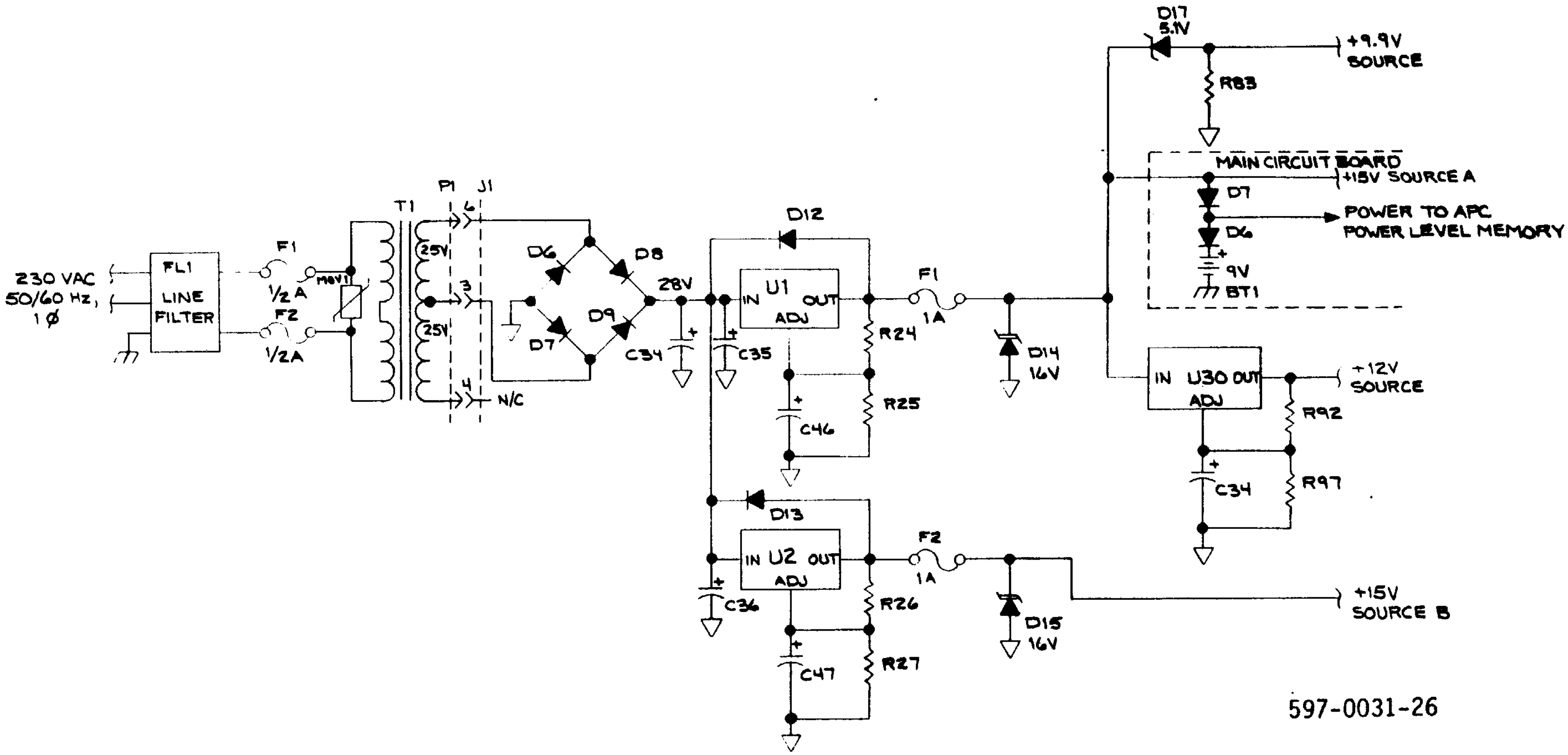

597–0031–26

FIGURE 1–2. APC POWER SUPPLY

1–21. Integrated circuit U1 is a three–terminal adjustable positive regulator containing internal thermal overload protection and short–circuit current limiting features. Overload protection for U1 is provided by fuse F1. Diode D14 protects the regulator from a reverse polarity potential applied to the output and provides transient suppression for all voltages exceeding 16 volts. Diode D12 protects the regulator from possible damage resulting from an input short.

1–22. A second supply connected to the output of U1 consists of regulator U30 which re–regulates the input into a 12 volt source which is applied to the **PRESET CAL** control and the 8–bit digital–to–analog converter on the main circuit board.

1–23. A third supply connected to the output of U1 consists of zener diode D17 and resistor R83. These components establish a 9.9 volt source which is used as a reference for precision current sources for the close–tolerance comparators on the main circuit board.

1–24. In case of power failures, the supply to the APC power level memory circuit will be maintained by a battery. Diode D7 prevents battery discharge through the APC circuitry during periods of battery operation and diode D6 isolates the 9 volt battery from the 15 volt A supply. Battery drain is approximately 0.8 microamperes which allows approximately two years of use (depending on the battery type). The battery is not maintained on charge and must be replaced when discharged.

1–25. **Positive Fifteen Volt Source B.** The power supply input potential is regulated into a 15 volt supply by U2. Capacitor C46 prevents regulator oscillation and C47 improves the response of the regulator. The output voltage is established by the value of resistors R26 and R27. The output of this supply operates all APC indicators and provides power for the APC output stages.

1–26. Integrated circuit U2 is a three–terminal adjustable positive regulator containing internal thermal overload protection and short–circuit current limiting features. Overload protection for U2 is provided by fuse F2. Diode D15 protects the regulator from a reverse polarity potential applied to the output and provides transient suppression for all voltages exceeding 16 volts. Diode D13 protects the regulator from possible damage resulting from input shorts.

1–27. APC LOGIC CIRCUITRY.

1–28. **MANUAL OPERATION.** Manual operation refers to operation of the transmitter with the automatic power control circuitry switched off (**APC ON** switch/indicator not illuminated). In this mode, RF power output is not automatically controlled, but responds only to manual raise and lower commands (see Figure 1–3).

1–29. When the APC unit is switched off, the Q output of U3A will go HIGH which selects the A inputs to the manual/automatic selector (U14). A HIGH through U7A and U9A will clear any preset power command. Fast speed correction is selected by a HIGH applied to analog switch U13B through U10A and U9C.

1–30. The local and remote raise power commands are applied to NOR gate U34C and the local and remote lower power commands are applied to NOR gate U34D. Each NOR gate will output the logical sum of its inputs. If the Q output of U3B is HIGH (remote disable), the remote inputs will be inhibited as one input of NOR gates U34A and U34B will be held HIGH.

1–31. The logic configuration used prevents simultaneous raise and lower commands. In event both commands are simultaneously initiated, U7B will give the lower power command priority over the raise power command by holding a HIGH on one input of NOR gate U7C.

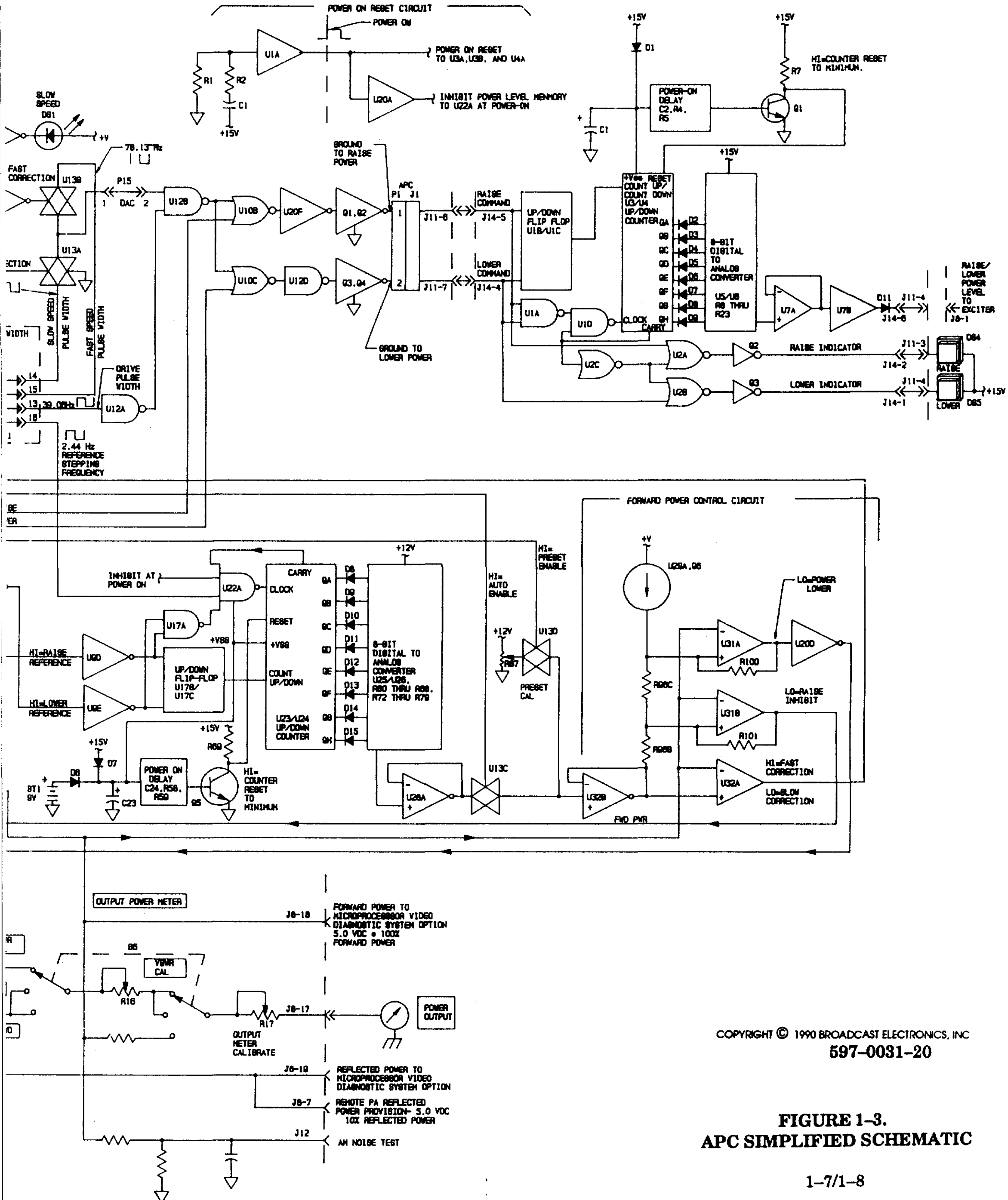

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FIGURE 1-3.
APC SIMPLIFIED SCHEMATIC

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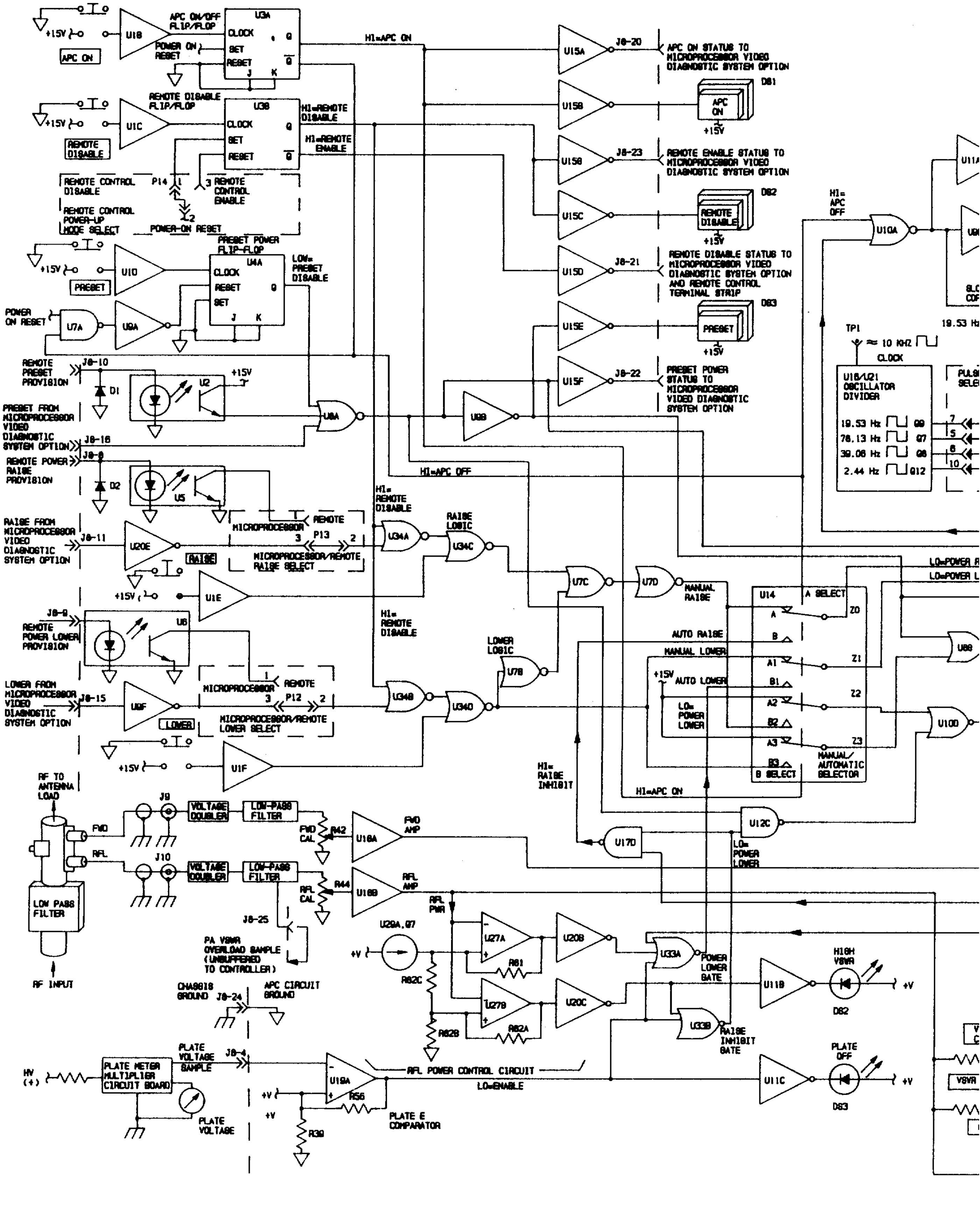


APC ON
APC ON/OFF FLIP/FLOP
U3A
CLOCK
SET
RESET
POWER ON RESET
HI=APC ON
APC ON STATUS TO MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION
REMOTE DISABLE
REMOTE DISABLE FLIP/FLOP
HI=REMOTE DISABLE
HI=REMOTE ENABLE
REMOTE ENABLE STATUS TO MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION
REMOTE CONTROL DISABLE
REMOTE CONTROL ENABLE
REMOTE CONTROL POWER-UP MODE SELECT
POWER-ON RESET
PRESET
PRESET POWER FLIP-FLOP
LOW= PRESET DISABLE
REMOTE DISABLE STATUS TO MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION AND REMOTE CONTROL TERMINAL STRIP
POWER ON RESET
REMOTE PRESET PROVISION
PRESET FROM MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION
PRESET POWER STATUS TO MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION
REMOTE POWER RAISE PROVISION
HI=APC OFF
HI= APC OFF
≈ 10 KHZ
CLOCK
U16/U21 OSCILLATOR DIVIDER
19.53 Hz
78.13 Hz
39.06 Hz
2.44 Hz
HI= REMOTE DISABLE
RAISE LOGIC
RAISE FROM MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION
MICROPROCESSOR
REMOTE
MICROPROCESSOR/REMOTE RAISE SELECT
RAISE
MANUAL RAISE
LO=POWER
A SELECT
AUTO RAISE
MANUAL LOWER
AUTO LOWER
LO= POWER LOWER
B SELECT
MANUAL/ AUTOMATIC SELECTOR
REMOTE POWER LOWER PROVISION
LOWER LOGIC
LOWER FROM MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION
MICROPROCESSOR/REMOTE LOWER SELECT
LOWER
HI= RAISE INHIBIT
HI=APC ON
RF TO ANTENNA LOAD
VOLTAGE DOUBLER
LOW-PASS FILTER
FWD CAL
FWD AMP
RFL CAL
RFL AMP
LO= POWER LOWER
LOW PASS FILTER
RF INPUT
RFL PWR
PA VSWR OVERLOAD SAMPLE (UNBUFFERED TO CONTROLLER)
POWER LOWER GATE
HIGH VSWR
RAISE INHIBIT GATE
CHASSIS GROUND
APC CIRCUIT GROUND
PLATE OFF
HV (+)
PLATE METER MULTIPLIER CIRCUIT BOARD
PLATE VOLTAGE SAMPLE
PLATE VOLTAGE
RFL POWER CONTROL CIRCUIT
LO=ENABLE
PLATE E COMPARATOR
VSWR

1–32. The raise or lower power command will be routed through U14 which functions as if it were a four–pole double–throw relay. In this situation, the "A" inputs will be routed to the outputs as follows:

Z0 will output a LOW if power raise was selected.

Z1 will output a LOW if power lower was selected.

Z2 will output a HIGH to U10D to prevent the power reference counter from counting down.

Z3 will output a HIGH to U8B to prevent the power reference counter from counting up.

1–33. A 78.13 Hz square wave is applied through analog switch U13B to one input of U12B. A 39.06 Hz square wave is applied to the second input to U12B from inverter U12A. The resultant logical sum of the inputs to U12B gates the power raise or power lower signal through U10B or U10C.

1–34. The power raise or power lower drive is then applied through an inverter to a Darlington stage. When there is no command to raise or lower power, both outputs will be HIGH. When there is a command to raise or lower power, the one output will go LOW.

1–35. When the output of a Darlington stage goes LOW, the resultant output of up/down flip–flop U1B/U1C will enable the up/down counter (U3/U4) to count up or count down. A HIGH from the flip–flop will enable the counter to count up. A LOW from the flip–flop will enable the counter to count down. Clock for the up/down counter is derived from the input signal via U1A and U1D. When the carry output of the up/down counter goes LOW, it will halt the clock and prevent the up/down counter from "rolling over" at maximum (1111 1111) or minimum (0000 0000) count.

1–36. During normal operation, transistor Q1 will be constantly energized. When power is applied to the transmitter, current will be applied to the up/down counter with Q1 off. This action will reset the up/down counter to minimum count, representative of minimum transmitter RF power output. After a short delay determined by the value of C2, R4, and R5, Q1 will energize and the reset line will go LOW to terminate the reset.

1–37. The up/down counter will begin to output eight–bit digital words as soon as input raise or lower command is applied. The eight–bit digital output of the up/down counter is converted to a dc level by the digital–to–analog converter consisting of U5, U6, and R8 through R23. This level is buffered by U7A and U7B and output as control voltage for the exciter.

1–38. The **RAISE** and **LOWER** indicators are driven by the raise and lower input commands. These commands are clocked through NOR gates U2A and U2B by inverted carry signal through NOR gate U2C. Q2 and Q3 function as output stages which apply a ground to one side of the appropriate indicator to illuminate the indicator.

1–39. **AUTOMATIC OPERATION.** When power is first applied to the APC, a high–going pulse will be generated by U1A which resets the command logic as follows. The duration of the pulse is determined by the value of C1, R1, and R2.

A. The APC on flip–flop (U3A) will be set to Q = HIGH to signify that the APC is on.

B. The remote disable flip–flop (U3B) will be set to the condition selected by the remote control power–up mode select jumper plug (P14). The following discussion will assume this jumper is set to disable remote control in which case Q = HIGH to signify remote control disable. The **REMOTE DISABLE** indicator will illuminate to signify that the remote control inputs are inhibited and additional outputs inform the optional microprocessor video display system of the remote control states, as well as a separate logic output on the remote control terminal block.

C. The preset power flip–flop (U4A) will be set to Q = LOW via NOR gate U7A and inverter U9A. This action will clear any preset power command at power–on.

D. Inverter U20A will hold a LOW on U22A to disable the power level memory inputs until power is fully energized.

1–40. The HIGH from U3A will inform the optional microprocessor video diagnostic system that the APC is enabled via U15A, illuminate the front–panel **APC ON** switch/indicator via U15B, and select the "B" inputs to the manual/automatic selector (U14).

1–41. The LOW from U4A will hold one input to NOR gate U8A LOW to disable the preset inputs. The HIGH from U8A will inform the optional microprocessor video diagnostic system that the preset power option is disabled via U15F, enable NOR gate U10D via U12C which allows raise memory reference, and enables the automatic level analog switch (U13C). The HIGH from U8A through inverter U9B will hold the front–panel **PRESET** switch/indicator off via U15E, disable the preset power analog switch (U13D), and enable NOR gate U8B which allows lower memory reference.

1–42. Normally, the power level memory battery (BT1) will always be installed and transistor Q5 will constantly be energized. When power is applied to the transmitter, current will be applied to the up/down counter (U23/U24). As the reset line to the up/down counter is normally held LOW by Q5, the count representative of the transmitter RF power output will be retained.

1–43. If, however, the power level memory battery is discharged, current will be applied to the up/down counter with Q5 off which resets the up/down counter to minimum count, representative of minimum transmitter RF power output. After a short delay determined by the value of C24, R58, and R59, Q5 will energize and the reset line will go LOW to terminate the reset.

1–44. During periods of battery operation, diode D7 prevents battery discharge through the power supply and diodes D8 through D15 prevent battery discharge through the digital to analog converter. The battery is not maintained on charge and is isolated from the power supply by diode D6. When the battery is discharged, it must be replaced with a new battery. The only circuitry backed–up by the battery is the up/down counter, composed of U22, U23 and U24.

1–45. Assuming that the up/down counter count has been retained, the up/down counter will begin to output eight–bit digital words as soon as the 2.44 Hertz clock is applied via U22A. The eight–bit digital output of the up/down counter is converted to a dc level by the digital–to–analog converter (U25/U26). This level is buffered by U28A and routed through analog switch U13C (which was selected when the **APC ON** switch was depressed) to voltage follower U32B.

1–46. If the count in the up/down counter was not preserved and was reset at power–on, the count must be manually re–established with the front–panel **RAISE** and **LOWER** switches.

1–47. The raise and lower command input circuit operates in a manner identical to that described by the manual operation discussion, however these inputs do not vary the APC output directly as in manual operation, but change the count stored in the up/down counter (U23, U24) which establishes the RF output level with a dc reference voltage.

1–48. The raise or lower power commands from the front–panel switches will be routed through U14 which functions as if it were a four–pole, double–throw relay. In this situation, the "B" inputs will be routed to the outputs as follows:

Z2 will output a LOW if power reference raise was manually selected.

Z3 will output a LOW if power reference lower was manually selected.

1–49. Any LOW from the Z2 output of U14 for power reference lower is applied through U10D to inverter U9D and bistable flip–flop U17B/ U17C. The second input of U10D will inhibit power reference raise if preset power has been selected or an abnormal operating condition is signaled by U33B.

1–50. Any LOW from output Z3 of U14 for power reference lower is applied through U8B to inverter U9E and bistable flip–flop U17B/U17C. The second input to U8B will inhibit power reference lower if preset power has been selected.

1–51. When the output of inverter U9D or U9E goes LOW, the resultant output of flip–flop U17B/U17C will enable the up/down counter to count up or count down. A HIGH from the flip–flop will enable the counter to count up. A LOW from the flip–flop will enable the counter to count down. U22A will toggle the clock of the up/down counter (U23/U24) when either a lower or raise reference command is passed by U17A. When the carry output of the up/down counter goes LOW, it will halt the clock and prevent the up/down counter from "rolling over" at maximum (1111 1111) or minimum (~~0000 0000~~) count.

1–52. **PA Forward Power Control Circuit.** Voltage follower U32B sinks current from constant current source U29A and Q6 to establish three precise voltages across the series string of resistors R96B and R96C. These voltages create dead–bands or windows which determine how the PA forward power control circuit will react when PA forward power increases beyond the level established by the input to U32B.

1–53. A sample of forward power from the PA forward meter amplifier (U18A) is applied to the inverting inputs of U31A, U31B, and U32A. If the PA forward power decreases to the extent that the level applied to the inverting input of U32A falls below the fixed reference on the non–inverting input of U32A, the output of voltage comparator U32A will change states and output a HIGH. This HIGH will force a LOW from U10A which is inverted by U9C to energize analog switch U13B for fast–speed correction. This allows fast correction where the forward power differs greatly from the fixed set–point.

1–54. In automatic operation, slow–speed and fast–speed correction is used. The lower frequency signal from U13A will provide slower correction as the clock rate is slower. The higher frequency signal from U13B will provide faster correction as the clock rate is faster.

1–55. As PA forward power increases to the proper level (approximately 90%), the level applied to the inverting input of U32A will rise above the fixed reference on the non–inverting input of U32A. The output of voltage comparator U32A will change states and output a LOW. This LOW will force a HIGH from U10A which energizes analog switch U13A for slow–speed correction. The HIGH from U10A will also illuminate the SLOW SPEED LED on the circuit board via U11A. U9C inverts this HIGH to deenergize analog switch U13B, the fast–speed gate.

1–56. If PA forward power then increases, the level on the inverting input of U31B will rise above the fixed reference on the non–inverting input of U31B. The output of voltage comparator U31B will change states and output a HIGH to U17D which inhibits further raise functions. This is the lower edge of the set–point "window", or dead–band. It is usually 1% to 2% below the desired power setting.

1–57. If the PA power should continue to increase to the point which is 1% to 2% above the desired setting, the level on the inverting input of U31A will rise above the fixed level on the non–inverting input of U31A and U31A will output a HIGH. This HIGH is inverted by U20D and applied as a LOW to U33A which lowers power.

1–58. As the PA power is lowered to the normal level, the potential on the inverting inputs of U31A and U31B will fall. First, U31A will return to a LOW output which removes the power lower command from U33A. The power will remain at this point within the set–point deadband. If the power should drop further, then U31B will return to a HIGH output which will output the raise command from U17D. The circuit will now function normally to control power, maintaining operation within the deadband.

1–59. The raise or lower power command will be routed through U14 which functions as if it were a four–pole, double–throw relay. In this situation, the "B" inputs will be routed to the outputs as follows:

Z0 will output a LOW via NAND gate U17D if automatic power raise is required. A LOW input to U17D from U33B will inhibit the raise function.

Z1 will output a LOW via NOR gate U33A if automatic power lower is required.

1–60. The remainder of the control circuitry functions in a manner identical to that described by the manual operation discussion.

1–61. **PA Reflected Power Control Circuit.** A sample of reflected power from the PA reflected meter amplifier (U18B) is applied to the inverting inputs of U27A and U27B.

1–62. Constant current source U29A/Q7 establishes two precise voltages across the series string of resistors R82C and R82B. The voltage across R82C creates a deadband or "window" which determines how the PA reflected power control circuit will react when PA reflected power increases beyond the level established by the reference on the non–inverting inputs of voltage comparators U27A and U27B.

1–63. The circuit will remain idle when the PA reflected power is below acceptable limits. If the PA reflected power increases and the level applied to the inverting input of U27B rises above the fixed reference on the non–inverting input of U27B (determined by the voltage across R82B), the output of voltage comparator U27B will change states and output a LOW. This LOW is applied as a HIGH to the raise inhibit gate (U33B) through inverter U20C to prevent PA power from increasing and illuminates the HIGH VSWR LED on the circuit board via inverter U11B. This prevents the forward power control circuit from raising power, preventing transmitter overload if a high VSWR exists.

1–64. If the PA reflected power continues to rise, the level on the inverting input of U27A will rise above the fixed reference on the non– inverting input and U27A will change states to output a LOW. This LOW is applied as a HIGH to the power lower gate (U33A) through inverter U20B to lower power. Thus, R82C establishes a "deadband" within which no raising or lowering power will occur.

1–65. When PA reflected power falls to a safe level and the level on the inverting input of U27A falls below the fixed reference on the non–inverting input, U27A will output a HIGH. This HIGH is applied as a LOW to U33A via U20B to halt the power reduction. However, the raise command will still be inhibited by U27B at the lower edge of the deadband.

1–66. If the PA reflected power continues to fall, the level on the inverting input of U27B will fall below the fixed reference on the non–inverting input and U27B will change states to output a HIGH. The resultant LOW from inverter U20C will enable U33B and allow power raise functions as required by the forward power control circuit. The automatic power control unit will then function normally again with full raise/lower control.

1–67. **Forward and Reflected Power Circuits.** The directional coupler located at the output end of the low–pass filter provides RF voltages proportional to the PA forward and reflected power. The reflected power sample is rectified by a voltage doubler (D2 and D4 on the rear panel circuit board), calibrated by R44, and amplified by U18B. The forward power sample is rectified by a voltage doubler (D1 and D3), calibrated by R42, and amplified by U18A. A low–pass filter after the rectifiers attenuates carrier envelope modulation caused by the power supply ripple and synchronous audio–rate amplitude modulation.

1–68. The reflected power signal is applied to the PA reflected power control circuit and the metering circuit. The forward power signal is applied to the PA forward power control circuit and the metering circuit. The metering information is applied to the **OUTPUT POWER METER** switch and displayed by the **OUTPUT POWER** meter. R17 provides a means to calibrate the **OUTPUT POWER** meter without affecting the set–up of the automatic system set by R42 and R44. This allows adjustment for routine calibration.

1–69. **Plate Voltage Monitor Circuit.** The soft start circuit monitors actual PA plate voltage. This circuit reduces the exciter output to minimum whenever plate voltage is off. Whenever the plate voltage is above the threshold, the circuit will gradually increase the exciter output until the rated transmitter RF output is established unless limited by a high VSWR condition, as gated by U33B.

1–70. A plate voltage sample derived from the plate meter multiplier circuit board is applied to the inverting input of voltage comparator U19A. When the plate voltage sample decreases below the fixed level (approximately 2.5 volts) on the non–inverting input of U19A established by R38 and R39 (such as when the high voltage power supply is off), U19A will output a HIGH. This HIGH will be applied to both the raise inhibit gate (U33B) and the lower power gate (U33A). U33B will inhibit the raise function and U33A will lower power to minimum. The HIGH from U19A will also illuminate the PLATE OFF LED on the circuit board via U11C. The power control element will stop lowering at minimum setting, but the lower command will remain present at the output of U33A through U12D.

1–71. When the **HIGH VOLTAGE ON** switch/indicator is depressed, the plate voltage sample from the plate meter multiplier circuit board will increase above the fixed reference on the non–inverting input and U19A will output a LOW. This LOW will remove the raise inhibit from U12C and U17D via U33B to raise power and will remove the power lower signal from U33A to allow the APC circuitry to re–establish transmitter RF power output as previously discussed.

1–72. **PRESET POWER.** As an additional function, a preset power level may be selected by the front–panel **PRESET** switch/indicator or activated with a continuous positive voltage connection to one of the APC preset power inputs (the APC must be enabled). This feature is normally used to automatically switch the transmitter to a predetermined power output level such as half–power for periods of auxiliary generator operation. The APC functions as before, only the internal power reference is manually adjusted by potentiometer R87.

NOTE   ***PRESET POWER IS ONLY USED FOR EMERGENCY OPERATION AT LESS THAN LICENSED POWER OPERATION. NO PROVISION TO REMOTELY ADJUST POWER IS PROVIDED IN THIS MODE.***

NOTE

1–73. The local, remote, and microprocessor video display system generated preset power inputs are applied to NOR gate U8A which outputs the logical sum of its inputs. If preset power is selected by any source, the output of U8A will be a HIGH. This HIGH accomplishes the following:

A. Deenergizes the automatic power control analog switch (U13C).

B. Disables NOR gate U10D via U12C to inhibit raise memory. Thus no change in the original APC power setting can occur if the **RAISE** switch is inadvertently depressed.

C. Informs the optional microprocessor video diagnostic system via U15F that the preset power function is energized.

D. Disables NOR gate U8B via U9B to inhibit lower memory. No change in the original APC power setting can occur if the **LOWER** switch is inadvertently depressed.

E. Energizes the preset analog switch (U13D).

F. Illuminates the front–panel **PRESET** switch/indicator via U15E as a local indication that the preset power function is energized.

1–74. The transmitter power output will now be determined by the setting of the preset cal potentiometer (R87) on the main circuit board. If power is removed from the APC unit, even momentarily, the preset power command will be automatically reset. The preset power mode will remain energized, however, if the remote input is connected to a voltage source.

BROADCAST ELECTRONICS, INC.

Appendix C

Typical Voltage and Current Overload Circuits
in
Contemporary Broadcast Transmitters

SECTION I
TRANSMITTER CONTROLLER THEORY OF OPERATION

1–1. **INTRODUCTION.**

1–2. The following text provides theory of operation with supporting diagrams for the FM–1B/FM–1.5B transmitter controller.

1–3. **FUNCTIONAL DESCRIPTION.**

1–4. Two levels of discussion are provided. A general discussion of the transmitter controller operation at block diagram level is followed by a detailed discussion of circuit operation.

1–5. **GENERAL DESCRIPTION.**

1–6. All status displays and most control functions in the FM–1.5B transmitter are implemented through use of a digital controller that monitors transmitter operation (see Figure 1–1). Using information collected throughout the transmitter, the controller will determine what control actions are required and complete these actions (such as timed intervals, overloads, or interlocks) without delay. The transmitter control logic will interface with most modern remote control devices and ATS units.

1–7. Information concerning overloads is presented by four front–panel indicators and stored for analysis after the problem has occurred to aid in problem resolution. Seven additional front–panel status indicators provide information relative to transmitter operation. Two internal LEDs indicate the transmitter power supply status and the controller overload and power–up memory battery status.

1–8. An optional diagnostic monitoring system utilizing a CRT display is available with the FM–1.5B transmitter. This microprocessor–based system continuously monitors and controls all major parameters of the transmitter and functions independently of the standard digital control circuit. Video displays of the transmitter operating conditions may be displayed in either an analog tabular chart format or a digital bar–graph format.

1–9. **OPERATION.**

1–10. The controller is constructed with solid–state digital circuitry on five circuit boards. The circuit boards are mounted within an enclosed chassis with a removable top for ease of maintenance. The RFI filter circuit board processes all inputs and outputs to minimize susceptibility to RF interference, the motherboard provides bus interconnections for the controller circuit board, and the controller circuit board provides logic functions. All the front–panel LED indicators are mounted on the front–panel indicator circuit board and all the front–panel switches are mounted on the front–panel switch circuit board. All operating potentials for the controller are provided by its own power supply. A fan ensures cool and reliable operation of the controller power supply.

1–11. Commands such as "filament on" and "high voltage on" are initiated by a momentary HIGH applied to conditional logic circuitry on the controller circuit board. A "one–button start" may be selected by depressing the **HIGH VOLTAGE ON** switch/indicator only. As each switch is depressed, the associated switch/indicator will illuminate to indicate that the selected command has been received and stored.

1–12. Assuming the **FILAMENT ON** and/or **HIGH VOLTAGE ON** switch/indicators have been depressed and all safety interlocks are closed, the blower will start. The safety–interlocks closed condition is signified by illumination of the front–panel **INTERLOCK** indicator.

1–13. When the air pressure switch closes, the **BLOWER** indicator will illuminate and the conditional logic will start the filament warm–up timer, apply filament voltage to the PA tube, and illuminate the **FILAMENT** indicator.

1–14. After the filament warm–up delay expires, if no overloads exist, all interlocks remain closed, and the air switch remains closed, a "high–voltage on" signal will be output to the high voltage step–start circuitry and remove the mute command from the FM exciter. The associated **HIGH VOLTAGE** indicator will illuminate to indicate that a "high voltage on command" has been output from the controller.

1–15. If the **HIGH VOLTAGE OFF** switch/indicator is depressed, a momentary HIGH applied to the conditional logic circuitry will deenergize the high voltage supply. When the **FILAMENT OFF** switch is depressed, a momentary HIGH applied to the conditional logic circuitry will deenergize the filament supply and initiate a filament cool–down interval. When the filament cool–down timer delay expires, the blower will deenergize. The **FILAMENT OFF** switch/indicator can be used to simultaneously deenergize both the plate and filament supplies if desired.

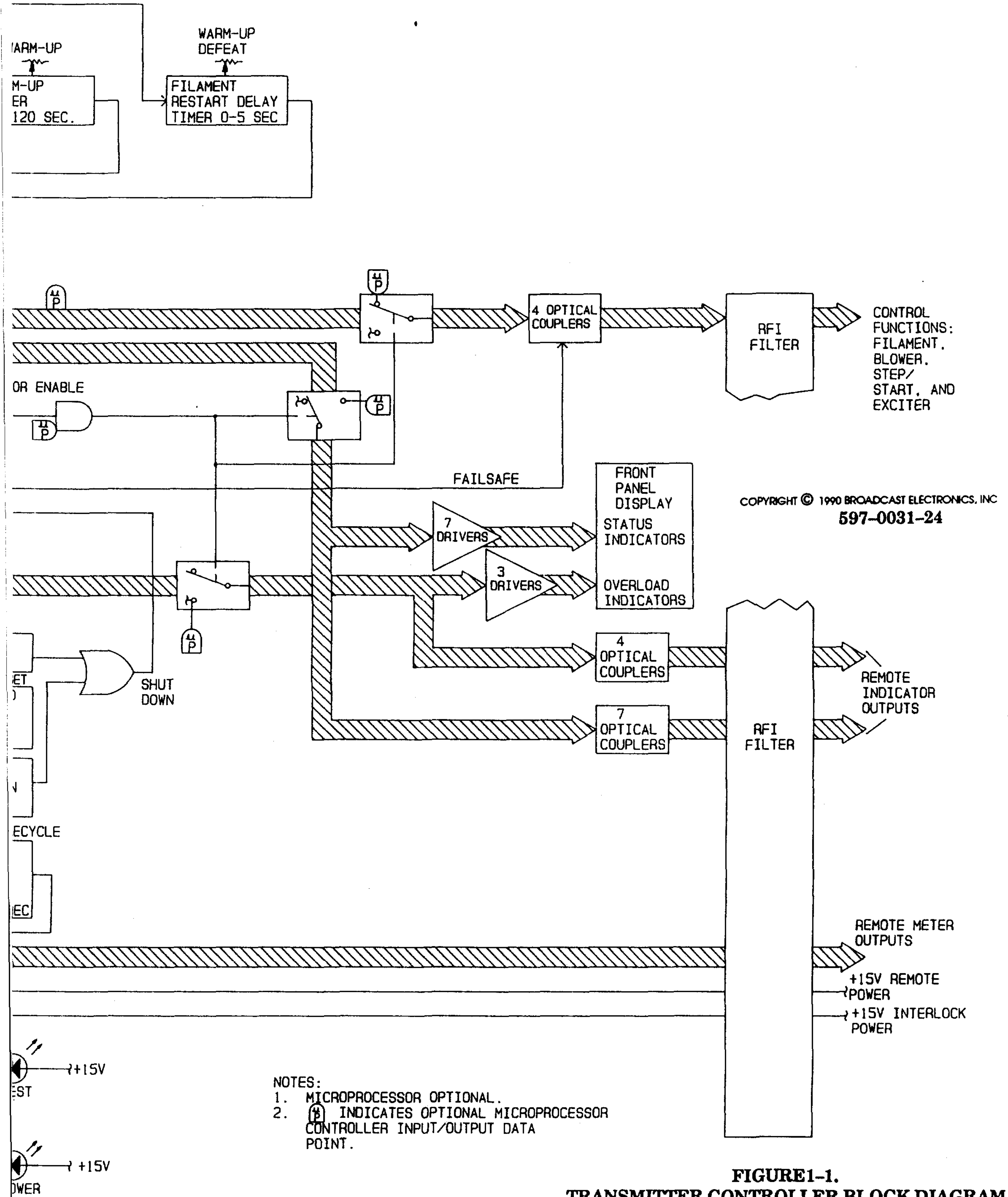
1–16. **REMOTE CONTROL.** Transmitter remote control is enabled whenever the automatic power control unit (APC) **REMOTE DISABLE** switch/indicator is not illuminated. Local control of the transmitter is possible at all times. The remote control inputs are routed through the controller RFI filter and coupled to the conditional logic circuitry in parallel with the local inputs through optical isolators. These optical isolators are enabled by a ground from the **APC REMOTE DISABLE** switch/indicator. Remote metering and status outputs are active at all times. A "one–button start" feature is incorporated as a remote control provision by using the high voltage on feature for one–button start and the filament off feature for one–button stop. All timing will be handled by the controller logic.

1–17. **INTERLOCKS.** If a safety interlock opens, the transmitter will deenergize immediately. The transmitter must be manually restored to operation after the open interlock is closed. The controller front–panel **INTERLOCK** indicator will go out to indicate an open interlock. If the opened safety interlock is closed before the filament cool–down timer interval expires, the blower will re–energize for the remaining duration of the cool–down cycle and then deenergize. If the air pressure interlock opens, the power supplies will deenergize immediately. When the interlock closes, the transmitter will return to operation automatically.

1–18. If the external interlock is opened, only the high voltage plate supply will be deenergized. The controller **HIGH VOLTAGE STATUS** indicator and the external interlock indicator (if installed) will extinguish to indicate an open interlock. When the external interlock is closed, the transmitter will return to operation automatically.

1–19. **OVERLOADS.** Plate current, control grid current, and PA reflected power are monitored for overload conditions. If an overload occurs, this information will be applied to the overload logic circuitry.

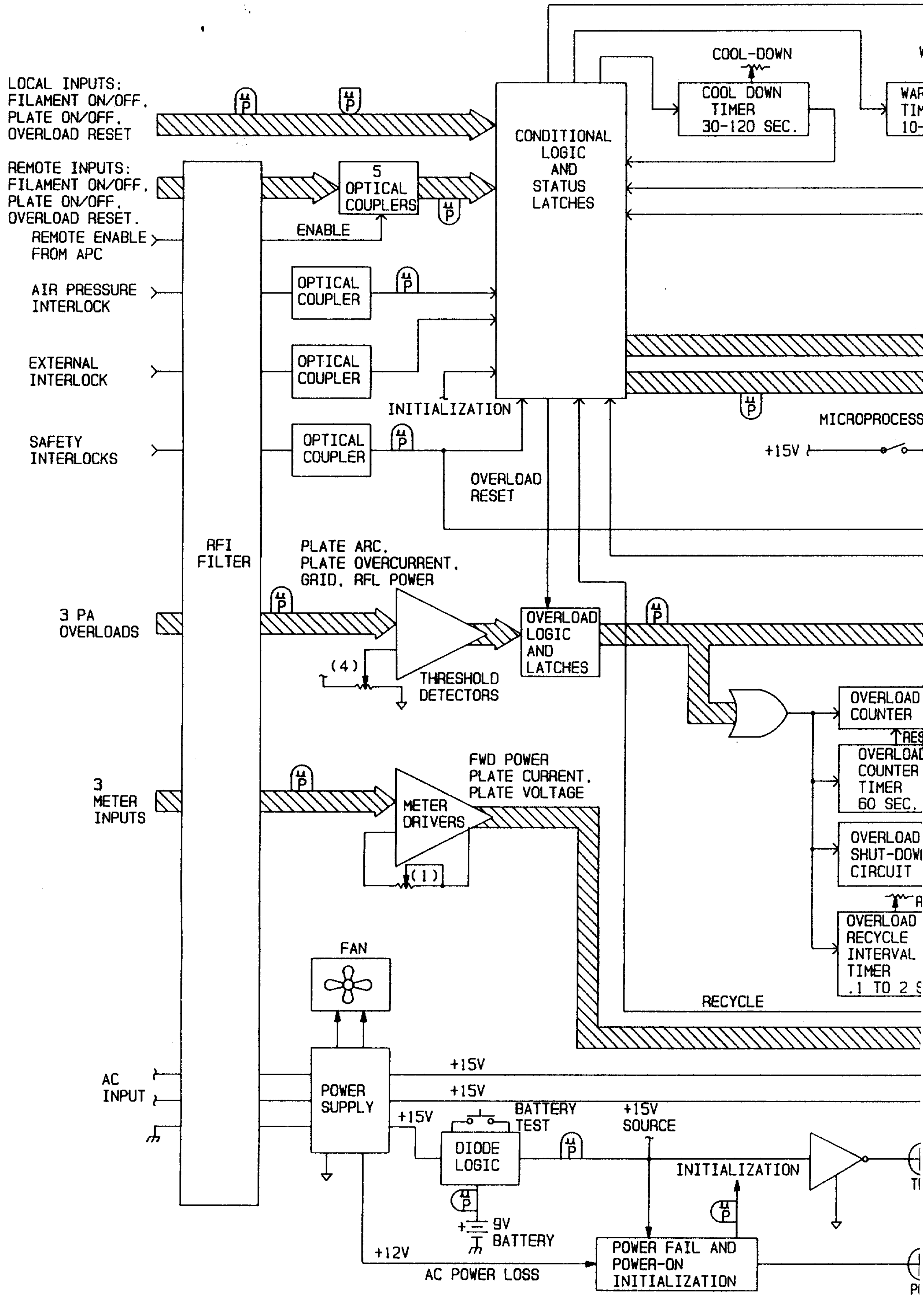
1–20. Any overload will illuminate the **OVERLOAD** indicator and initiate two timed intervals. A timer/counter pair monitors the number of times an overload occurs during a 60 second interval and the second timer delays restoration of the transmitter to operation to allow the condition that prompted the overload to dissipate.



NOTES:
1. MICROPROCESSOR OPTIONAL.
2. µP INDICATES OPTIONAL MICROPROCESSOR CONTROLLER INPUT/OUTPUT DATA POINT.

597-0031-24

FIGURE 1-1.
TRANSMITTER CONTROLLER BLOCK DIAGRAM



LOCAL INPUTS:
FILAMENT ON/OFF,
PLATE ON/OFF,
OVERLOAD RESET
REMOTE INPUTS:
FILAMENT ON/OFF,
PLATE ON/OFF,
OVERLOAD RESET.
REMOTE ENABLE
FROM APC
AIR PRESSURE
INTERLOCK
EXTERNAL
INTERLOCK
SAFETY
INTERLOCKS
3 PA
OVERLOADS
3
METER
INPUTS
AC
INPUT
RFI
FILTER
5
OPTICAL
COUPLERS
ENABLE
OPTICAL
COUPLER
OPTICAL
COUPLER
OPTICAL
COUPLER
INITIALIZATION
OVERLOAD
RESET
CONDITIONAL
LOGIC
AND
STATUS
LATCHES
COOL-DOWN
COOL DOWN
TIMER
30-120 SEC.
MICROPROCESS
+15V
PLATE ARC,
PLATE OVERCURRENT,
GRID, RFL POWER
(4)
THRESHOLD
DETECTORS
OVERLOAD
LOGIC
AND
LATCHES
OVERLOAD
COUNTER
OVERLOAD
COUNTER
TIMER
60 SEC.
OVERLOAD
SHUT-DOW
CIRCUIT
OVERLOAD
RECYCLE
INTERVAL
TIMER
.1 TO 2 S
RECYCLE
FWD POWER
PLATE CURRENT,
PLATE VOLTAGE
METER
DRIVERS
(1)
FAN
POWER
SUPPLY
+15V
+15V
+15V
BATTERY
TEST
+15V
SOURCE
DIODE
LOGIC
INITIALIZATION
9V
BATTERY
+12V
AC POWER LOSS
POWER FAIL AND
POWER-ON
INITIALIZATION

1–21. When the timed interval delaying restoration of the transmitter to operation has expired, the transmitter will recycle back into operation. If no further overloads occur during the 60 second interval following the first overload, the 60 second timer will clear the overload counter. If four overload recycles occur during the 60 second counter/timer interval, the transmitter will deenergize and must be manually reset. This can be done by depressing the **OVERLOAD** switch/indicator, the **FILAMENT ON** switch/indicator, and the **HIGH VOLTAGE ON** switch/indicator. The overload can also be cleared by remote control if remote control is enabled by the **APC REMOTE DISABLE** switch/indicator.

1–22. If an overload persists in duration for longer than 0.22 seconds, the overload shut–down circuit will consider the overload a short circuit and immediately deenergize the transmitter. The transmitter must then be manually restored to operation after the fault is repaired.

1–23. **DETAILED DESCRIPTION.**

1–24. **RFI FILTER CIRCUIT BOARD.** All controller inputs and outputs are routed through connectors J1, J2, and J3 mounted to the RFI filter circuit board. The circuitry consists of single PI–section low–pass RC and LC filters effective to 108 MHz and connected in series with each input and output to prevent RF leakage into the controller. The filter circuit board also contains the following programmable circuitry: 1) inverter arrays U1 and U2 which determine the remote status indication logic, 2) resistor network R35 which functions as a voltage divider to reduce the remote meter indications to +2.5V dc, and 3) jumper J7 which selects either independent or safety external interlock operation.

1–25. **MOTHERBOARD.** The motherboard provides a single 100–pin edge connector (J1) to mount the controller circuit board. Logic inputs and outputs to the motherboard are routed via ribbon cables and connected to J3 and J4. Power is connected to J2.

1–26. **CONTROLLER CIRCUIT BOARD.** Input latches U17A, U17B, and U17C are used to store the momentary contact closures representative of command inputs (see Figure 1–2). When the **FILAMENT ON** switch/indicator is depressed, a momentary LOW from NOR gate U9A will force the Q output of U17A HIGH. When the **HIGH VOLTAGE ON** switch/indicator is depressed, a momentary LOW from NOR gate U10A will force the Q output of U17B HIGH. A "one–button start" feature is provided by a connection from the Q output of U17B to U9A.

1–27. **Blower On.** The HIGH from the Q output of U17A is applied to the blower off delay circuit, analog switch U32, blower timer U23A and filament gate U19A. The blower off delay circuit has no function at transmitter turn–on. The input to analog switch U32 illuminates the **FILAMENT ON** switch/indicator to signify that the filament on command has been received and stored. A HIGH from the Q output of blower timer U23A will be applied to blower AND gate U26A through OR gate U24A. Assuming the safety interlocks remain closed, the remaining input to U26A will be HIGH and a HIGH will be output through analog switch U32 and optical isolator U38 to energize the blower control circuitry.

1–28. The output potential for optical isolator U38 is routed through the safety interlocks. If the safety interlock string opens, the blower control voltage will be disconnected and the safety interlock control logic will completely deenergize the transmitter.

1–29. **Filament On.** As the blower continues to operate, the air switch will close. The air switch closed signal is applied to optical isolator U6 which forces a HIGH from U12B and a LOW from U12C. The LOW from U12C is applied to inverter U18A which will output a HIGH to filament AND gate U19A. As the remaining input to U19A was set HIGH by the Q output of U17A, a HIGH will be output through analog switch U34 and optical isolator U37 to activate the filament circuit. The **FILAMENT** status indicator will illuminate to signify that the filament circuit is energized.

1–30. The output potential for optical isolator U37 is routed through the safety interlocks. If the safety interlock string opens, the filament control voltage will be disconnected and the safety interlock control logic will completely deenergize the transmitter.

1–31. **High Voltage On.** Assuming the **HIGH VOLTAGE ON** switch/indicator has been depressed, a HIGH from the Q output of U17B through analog switch U32 will illuminate the **HIGH VOLTAGE ON** switch/indicator to signify the high voltage on command has been received and stored. The previously set HIGH from U19A (the filament gate) will also be applied to the filament on delay and gate U14B.

1–32. If the ac power status input to U14B is HIGH, AND gate U14B will output a HIGH to start filament timer U23B. The output of U23B will start HIGH, go LOW for the duration of the filament heating delay, then return HIGH. The filament on delay circuit will hold a momentary LOW on high voltage gate U25A to prevent the time delay encountered in starting timer U23B from pulsing the high voltage circuit on, then off, then back on after the filament heating delay.

1–33. When the filament heating delay has expired and a HIGH from U19B signals that no overloads exist, U25A will output a HIGH to U34. U34, operating in conjunction with inverter U51C will output a LOW to step–start OR gate U24B. If a LOW from the external interlock circuit is present (indicating the interlock is closed), U24B will output a LOW to energize the step–start circuit.

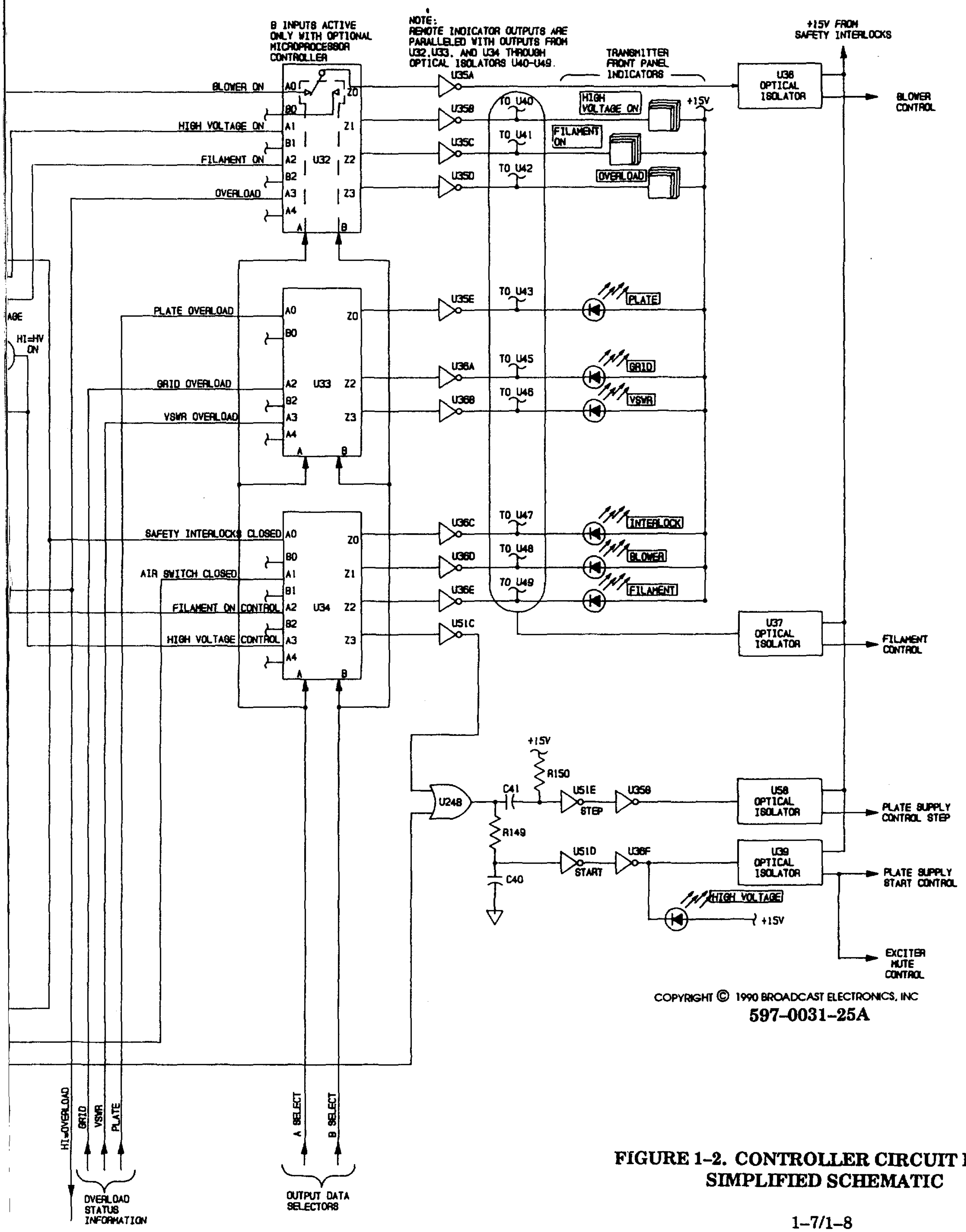
1–34. The step driver will energize the plate supply step relay to apply primary voltage to the plate supply transformer through three limiting resistors. After a 100 millisecond delay determined by R149, C40, and U51D, the start driver will energize the start contactor and apply the full primary potential to the plate supply transformer. The step circuit will deenergize after being energized for 160 milliseconds, determined by R150, C41, and U51E. In this manner, the plate supply in–rush is limited and the current limiting resistors are subject to heating only during a 100 millisecond interval before start contactor closure. For added reliability, the limiting resistors are disconnected after 160 milliseconds.

1–35. The exciter enable line and the **HIGH VOLTAGE** status indicator are wired in parallel from U39 with the start driver. Simultaneous with generation of the start signal, the exciter will be enabled and the **HIGH VOLTAGE** status indicator will illuminate to indicate that the plate supply control signal has been output. The high voltage supply is prevented from step–starting under full load in this manner.

1–36. The output potential for optical isolator U39 is routed through the safety interlocks. If the safety interlock string opens, the plate supply start control voltage will be disconnected and the safety interlock control logic will completely deenergize the transmitter.

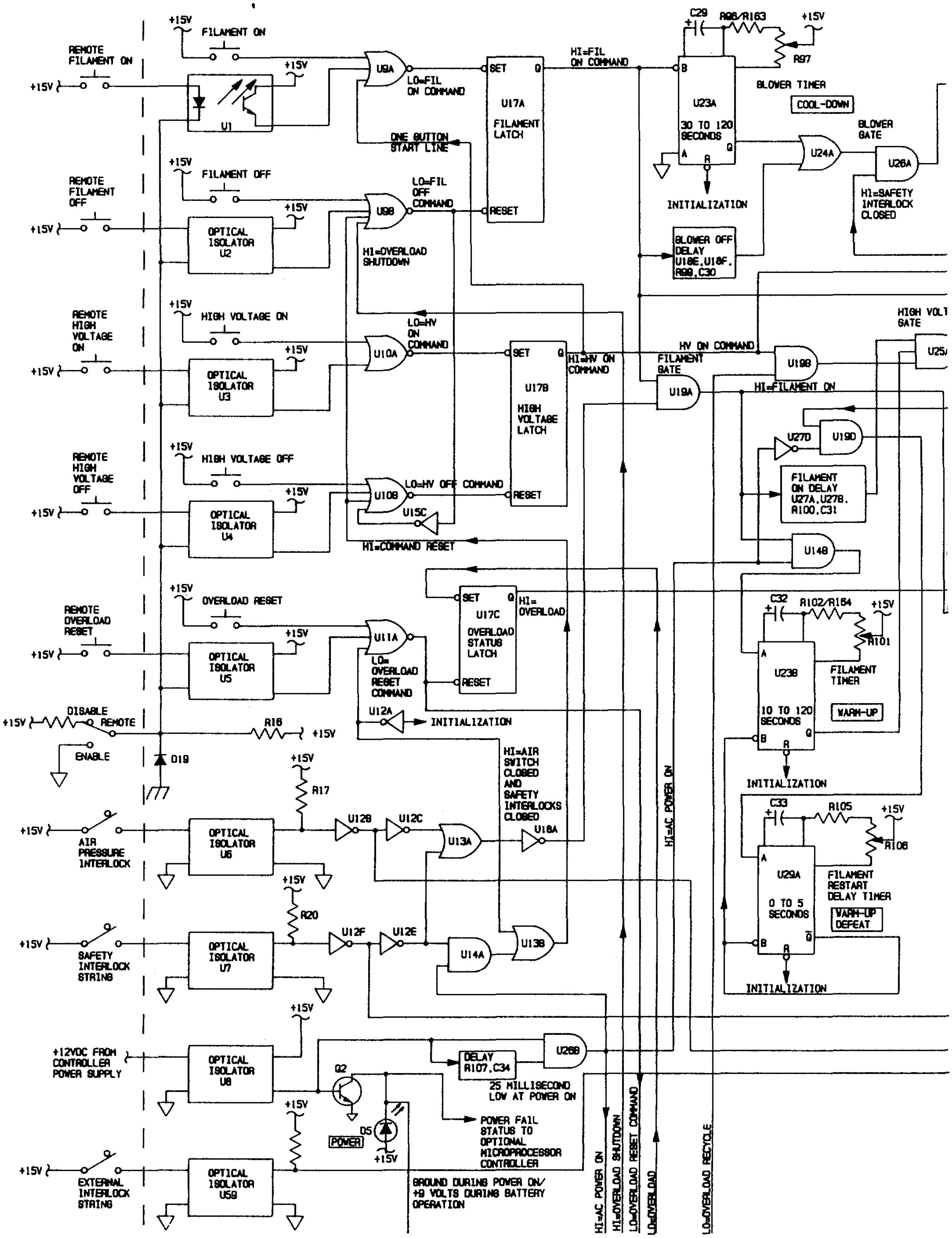
1–37. **Power–On Initialization.** When power is initially first applied to the transmitter controller circuit board, the +15 volt input to inverter U18B through R98 will produce a LOW output from U18B which clears all timers and resets all latches to the off condition. Capacitor C13 will gradually charge from the +15 volt dc input through resistor R24. When the charge on C13 equals the 2 volt threshold established by D3, D4, and Q1, transistor Q1 will conduct and force a HIGH from inverter U18B which will terminate the power–on initialization. Q1 will remain conducting as long as power is continuously applied to the +15 volt input.

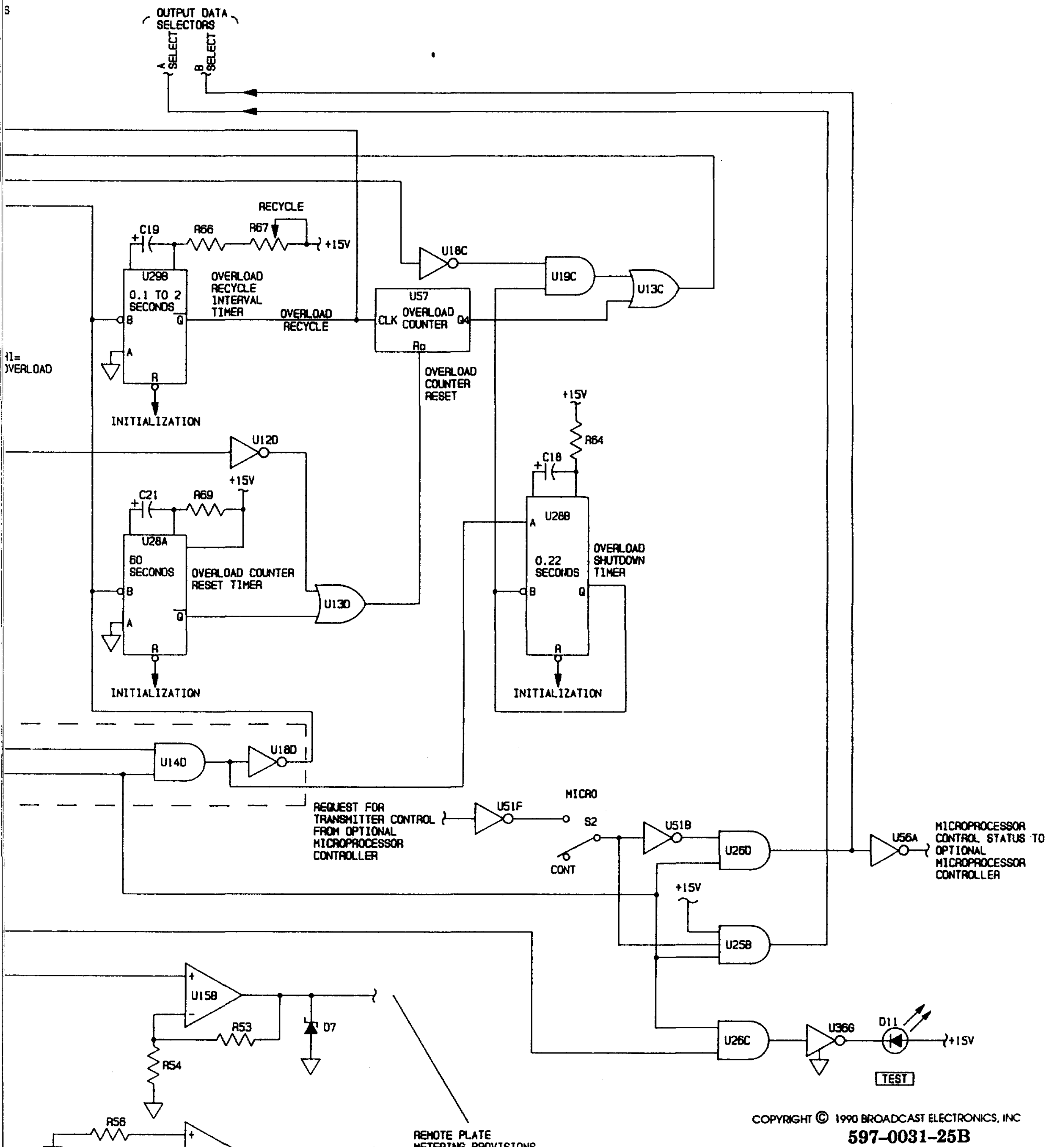
1–38. Initialization is also applied to inverter U12A. U12A outputs a HIGH which resets the overload status latch (U17) via U11A, resets the overload latches (U31A, U31C, and U31D), and resets the overload counter (U57) through inverter U12D. The HIGH from U12A is also applied through OR gate U13B to U9B and U10B to reset the filament latch and the high voltage latch.



597-0031-25A

FIGURE 1-2. CONTROLLER CIRCUIT BOARD SIMPLIFIED SCHEMATIC

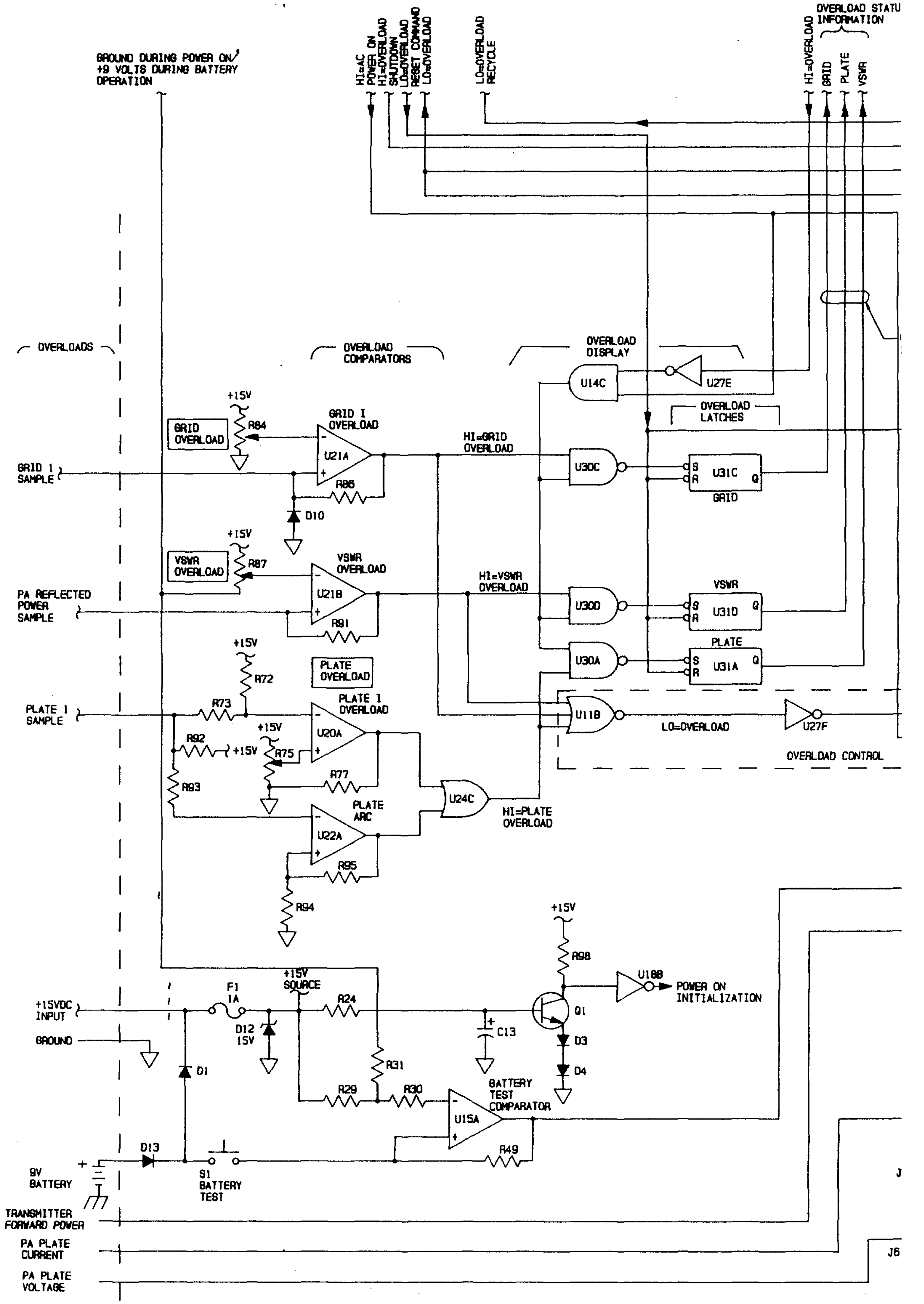

REMOTE FILAMENT ON
FILAMENT ON
+15V
U1
U9A
LO=FIL ON COMMAND
SET Q
U17A
FILAMENT LATCH
RESET
HI=FIL ON COMMAND
ONE BUTTON START LINE
C29
R96/R163
R97
B
U23A
30 TO 120 SECONDS
A R Q
BLOWER TIMER
COOL-DOWN
BLOWER GATE
U24A
U26A
HI=SAFETY INTERLOCK CLOSED
INITIALIZATION
BLOWER OFF DELAY U18E,U18F, R99,C30
REMOTE FILAMENT OFF
FILAMENT OFF
LO=FIL OFF COMMAND
U9B
OPTICAL ISOLATOR U2
HI=OVERLOAD SHUTDOWN
REMOTE HIGH VOLTAGE ON
HIGH VOLTAGE ON
LO=HV ON COMMAND
U10A
OPTICAL ISOLATOR U3
U17B
HIGH VOLTAGE LATCH
HI=HV ON COMMAND
HV ON COMMAND
FILAMENT GATE
U19A
U19B
HIGH VOLT GATE
U25A
HI=FILAMENT ON
U27D
U19D
FILAMENT ON DELAY U27A,U27B, R100,C31
REMOTE HIGH VOLTAGE OFF
HIGH VOLTAGE OFF
U10B
LO=HV OFF COMMAND
OPTICAL ISOLATOR U4
U15C
HI=COMMAND RESET
U14B
REMOTE OVERLOAD RESET
OVERLOAD RESET
U11A
LO= OVERLOAD RESET COMMAND
OPTICAL ISOLATOR U5
U17C
OVERLOAD STATUS LATCH
HI= OVERLOAD
C32
R102/R164
R101
U23B
10 TO 120 SECONDS
FILAMENT TIMER
WARM-UP
DISABLE
REMOTE
ENABLE
U12A
INITIALIZATION
R16
D19
R17
HI=AIR SWITCH CLOSED AND SAFETY INTERLOCKS CLOSED
HI=AC POWER ON
AIR PRESSURE INTERLOCK
OPTICAL ISOLATOR U6
U12B
U12C
U13A
U18A
C33
R105
R106
U29A
0 TO 5 SECONDS
FILAMENT RESTART DELAY TIMER
WARM-UP DEFEAT
R20
SAFETY INTERLOCK STRING
OPTICAL ISOLATOR U7
U12F
U12E
U14A
U13B
+12VDC FROM CONTROLLER POWER SUPPLY
OPTICAL ISOLATOR U8
U26B
DELAY R107,C34
25 MILLISECOND LOW AT POWER ON
Q2
D5
POWER
POWER FAIL STATUS TO OPTIONAL MICROPROCESSOR CONTROLLER
EXTERNAL INTERLOCK STRING
OPTICAL ISOLATOR U59
GROUND DURING POWER ON/ +9 VOLTS DURING BATTERY OPERATION
HI=AC POWER ON
HI=OVERLOAD SHUTDOWN
LO=OVERLOAD RESET COMMAND
LO=OVERLOAD
LO=OVERLOAD RECYCLE



597-0031-25B

FIGURE 1-2. CONTROLLER CIRCUIT BOARD SIMPLIFIED SCHEMATIC

BROADCAST ELECTRONICS INC


GROUND DURING POWER ON/
+9 VOLTS DURING BATTERY
OPERATION
HI=AC
POWER ON
HI=OVERLOAD
SHUTDOWN
LO=OVERLOAD
RESET COMMAND
LO=OVERLOAD
LO=OVERLOAD
RECYCLE
OVERLOAD STATU
INFORMATION
HI=OVERLOAD
GRID
PLATE
VSWR
OVERLOADS
OVERLOAD
COMPARATORS
OVERLOAD
DISPLAY
U14C
U27E
OVERLOAD
LATCHES
+15V
R84
GRID
OVERLOAD
GRID I
OVERLOAD
U21A
R86
HI=GRID
OVERLOAD
U30C
S
R
U31C
Q
GRID
GRID 1
SAMPLE
D10
+15V
VSWR
OVERLOAD
R87
VSWR
OVERLOAD
U21B
R91
HI=VSWR
OVERLOAD
U30D
VSWR
U31D
PA REFLECTED
POWER
SAMPLE
+15V
R72
PLATE
OVERLOAD
U30A
PLATE
U31A
PLATE I
OVERLOAD
PLATE 1
SAMPLE
R73
U20A
+15V
R92
+15V
R75
U11B
LO=OVERLOAD
U27F
OVERLOAD CONTROL
R77
R93
U24C
PLATE
ARC
HI=PLATE
OVERLOAD
U22A
R95
R94
+15V
R98
U18B
POWER ON
INITIALIZATION
+15V
SOURCE
F1
1A
R24
+15VDC
INPUT
Q1
D12
15V
C13
GROUND
D3
D4
D1
R31
R29
R30
BATTERY
TEST
COMPARATOR
U15A
R49
D13
9V
BATTERY
S1
BATTERY
TEST
J
TRANSMITTER
FORWARD POWER
PA PLATE
CURRENT
J6
PA PLATE
VOLTAGE

1–39. **AC Power Monitor.** A +12 volt dc input from the controller power supply is monitored for instantaneous loss of ac power information. This input to optical isolator U8 will drive transistor Q2 into conduction which illuminates the **POWER** indicator. U8 also forces a HIGH from U26B which signifies ac power is applied to the transmitter. A 25 millisecond delay connected to the second input of U26B will delay the HIGH from U26B to allow all logic adequate time to reset before signaling ac power has returned to normal.

1–40. The ac power status information from U26B is ANDed in U14A with the safety interlock status. If the safety interlocks are opened while ac power is energized, a HIGH from U14A will be applied through OR gate U13B to U9B and U10B to reset the filament latch and the high voltage latch.

1–41. When the output of U26B is LOW (ac power lost), several actions occur:

A. The filament restart delay timer (U29A) is set via U19D as soon as ac power is lost. If ac power is removed long enough for the filament restart delay timer interval to expire, U29A will reset the filament timer. When power returns, a new filament heating delay will be initiated before the plate supply is energized. If the ac power outage is momentary and U29A is not allowed to time out, high voltage will energize immediately upon restoration of ac power.

B. The overload comparators and latches will be inhibited by U30 as any inputs during power off will be false.

C. Additional circuitry inhibits the battery **TEST** indicator to conserve battery current, selects the A inputs to the analog switches for solid–state controller operation only, and advises the optional microprocessor controller of battery operation status.

1–42. The collector of Q2 routes power failure information to the optional microprocessor controller and provides a ground reference when ac power is on for VSWR overload control R97, and battery test comparator U15A. During periods of battery operation, this same line routes a positive potential to the VSWR overload reference control. This eliminates false overloads on ac power failure due to a slowly decaying VSWR sample.

1–43. **Safety Interlocks.** The safety interlock circuitry consists of a series string of normally closed switches mounted in areas which contain electrical or mechanical hazards. Each switch is mechanically activated by a door or panel to deenergize the entire transmitter when opened. Logic states from the safety interlock circuitry are used in conditional logic for blower and filament turn on as described in the following text.

1–44. All outputs from the controller are routed through optical isolators. The output potential for the optical isolators is obtained from the series–wired safety interlock string. If an interlock opens, all output drivers from the controller circuit board will be disconnected. In addition, the safety interlock control logic input will be removed and the transmitter will completely deenergize.

1–45. The safety interlock closed information is input to optical isolator U7 and applied to inverter U12F as a LOW. When HIGH, the output of U12F will illuminate the **INTERLOCK** status indicator through analog switch U34 to signify the interlocks are closed and enable blower gate U26A.

1–46. The HIGH from U12F is also applied as a LOW to OR gate U13A and AND gate U14A through inverter U12E. OR gate U13A enables the filament gate (U19A) to allow filament turn–on. When both inputs to U13A are LOW, U13A will output a LOW to inverter U18A which applies a HIGH to the filament AND gate. This will occur whenever both the air pressure and the safety interlock switches are closed. AND gate U14A will produce the logical sum of a LOW from the safety interlock circuit and a HIGH from the ac power monitor circuit. If the safety interlocks are opened while ac power is applied to the transmitter, a HIGH through U13B will reset the filament latch via U9B and the high voltage latch via U10B to deenergize the transmitter. This will prevent the transmitter from re–energizing the filament or high voltage circuit upon closing the open interlock condition. Only the blower run–down timer (U23A) is allowed to continue operation.

1–47. **External Interlock.** The external interlock circuit is independent of the transmitter safety interlock circuit. External interlock closed information is applied to optical isolator U59 as a HIGH. The output of U59 will pull one input of step–start control OR gate U24B LOW, allowing a control pulse from U51C to enable the step–start circuitry. If the interlock is opened during transmitter operation, a HIGH is applied to U24B which disables the high voltage step–start circuit and deenergizes the plate supply.

1–48. **Overload Input Circuit.** Three parameters are monitored for overload conditions by the controller circuit board: control grid current, PA VSWR, and plate current. Each sample is input to a threshold comparator which converts the analog input to a digital state. Depending upon the polarity of the sample, the input is applied to the inverting or non–inverting input of the comparator. Resistors R92 and R72 on the plate sample form voltage dividers with the series input resistors (R93 and R73) to convert the negative samples to positive voltages for the comparators. An adjustable threshold is established on the remaining input to each comparator. When the sample crosses the preset threshold, the output will switch from a LOW to a HIGH to signal an overload condition. The grid current overload will trip on excessive drive.

1–49. Two comparators are used to monitor the plate current sample. The slower overload comparator (U20A) monitors for gradual increases such as mistuning which can draw up to two times normal plate current. The plate arc comparator (U22A) is a faster operating circuit that monitors for high–level short–duration arcs which will not trigger U20A. The two plate overload comparators are ORed in U24C. A HIGH from U24C signals a plate overload.

1–50. All four comparators normally output a LOW and switch to a HIGH to signal an overload condition. This logic is used as inputs for the overload display as well as the overload control circuitry.

1–51. **Overload Diagnostics.** For diagnostic display purposes, the output of each comparator is ANDed with a comparator enable signal and latched into a bistable flip–flop. Immediately after an overload is latched, the display enable signal will go LOW and inhibit further inputs. Until cleared with the overload **RESET** switch, no further overload information will be accepted for diagnostic display purposes. Any overload will be output from the latches as a HIGH through analog switch U33 for display as a diagnostic indication.

1–52. The overload latch (U17C) is set by a LOW from inverter U18D. A HIGH from the Q output of U17C will illuminate the **OVERLOAD** switch/indicator to signify that an overload has occurred. The HIGH from U17C is also inverted by U27E and ANDed in U14C with the ac power status to disable the overload latches (U31A, U31C, and U31D) through U30A, U30C, and U30D, inhibiting further overload inputs to the latches. The overload latch that was set by the overload input will illuminate its respective front–panel indicator via U33.

1–53. The overload display reset sequence is initiated by a positive potential which resets overload status latch U17C through NOR gate U11A. When U17C is reset, several actions occur:

A. The **OVERLOAD** reset switch/indicator and the overload diagnostic indicator (**PLATE, GRID**, or **VSWR**) indicator will go out.

B. The overload display latches (U31A, U31C, and U31D) will be reset.

C. The inhibit from U14C will be removed from the overload display gates.

D. The overload counter will be cleared via inverter U12D and OR gate U13D.

1–54. **Overload Control Circuits.** The overload control circuit inputs are obtained from the overload comparators. This circuit is not inhibited by a single overload as is the overload display circuit. The logical output of each comparator is ORed in U11B, routed through inverter U27F, and ANDed with the ac power status in U14D. An output from U14D is applied as a HIGH to overload shutdown timer U28B. This timer measures the duration of the high overload signal. If it is greater than 220 milliseconds, it applies a signal through U19C and U13C to deenergize filament latch U17A via U9B. This same HIGH is routed through inverter U18D and applied as a LOW to enable the overload counter reset timer (U28A), enable the overload recycle interval timer (U29B), and set the overload status latch (U17C).

1–55. The overload recycle interval timer (U29B) determines the length of time the transmitter remains off–the–air after an overload to allow the condition that prompted the overload to dissipate. Timer U29B can be adjusted from 0.1 to 2 seconds using R67. The overload counter (U57) counts the overload recycle attempts and the overload counter reset timer (U28A) resets the overload counter 60 seconds after the first overload occurred.

1–56. Each overload will initiate a recycle by deenergizing high voltage via AND gates U19B and U25A to attempt to clear the overload. The overload counter (U57) will count each recycle attempt. If four overloads occur within the 60 second interval of U28A, OR gate U13C will output a HIGH. This HIGH is applied to OR gate U9B which resets the filament latch (U17A) and deenergize the transmitter.

1–57. If an overload cycles the transmitter off–the–air and removing high voltage does not clear the overload after 220 milliseconds, the overload shutdown timer (U28B) will output a HIGH. This HIGH is ANDed in U19C with a HIGH from inverter U18C and signals overload shut–down through OR gate U13C.

1–58. **Turn Off.** The high voltage off sequence is initiated by a positive potential which resets the high voltage latch (U17B) through NOR gate U10B. When U17B is reset, the following actions will occur:

A. The **HIGH VOLTAGE ON** switch/indicator will go out.

B. A LOW via U19B and U25A will deenergize the plate power supply and the **HIGH VOLTAGE** status indicator will go out.

1–59. The filament off sequence is initiated by a positive potential which resets the filament latch (U17A) through NOR gate U9B. When U17A is reset, the following actions will occur:

A. The plate latch (U17B) will be reset by U10B via U9B.

B. The **FILAMENT ON** switch/indicator will go out.

C. A LOW via U19A will deenergize the filament supply and the **FILAMENT** status indicator will go out.

D. The blower timer (U23A) will begin time–down operation. The blower–off delay circuit composed of U18E, U18F, C30, and R99 will hold a momentary HIGH through U24A on blower gate U26A to prevent the time delay encountered in starting timer U23A from pulsing the blower off, then on, then back off after the blower run–down delay.

E. When the blower ceases operation, the **BLOWER** status indicator will go out.

1–60. **Remote Control.** The transmitter can be controlled by momentary positive–polarity dc inputs to the controller circuit board. Positive–logic enabled remote inputs are used for safety. Each remote input is routed through an optical isolator for isolation. Additional resistance to noise interference is provided by an RC circuit in each remote input. Diodes across each optical isolator input and diode D19 prevent possible damage to the remote circuitry caused by inadvertent connection to negative polarity control inputs. A +15 volt output is provided for remote operation, however the optical isolators can operate on any positive dc voltage from +5 volts to +24 volts.

1–61. The remote circuitry is enabled by a ground through the **REMOTE ENABLE/DISABLE** switch which enables the optically–isolated inputs. The input of this switch is connected to a pull–up resistor (R16) as a safety consideration to prevent remote operation in case the switch input were to become disconnected.

1–62. **Remote PA Metering.** The remote meter amplifiers for transmitter forward power, PA plate current, and PA plate voltage are mounted on the controller circuit board.

1–63. U15B is a non–inverting voltage amplifier with a gain of approximately one and used for transmitter forward power. The input is obtained from the forward power buffer in the automatic power control unit. The output is clamped with a 15 volt zener diode for circuit protection. Positive five volts output corresponds to 100% power.

1–64. U16A is an inverting voltage amplifier with a gain of approximately 12. The input is obtained from one end of a resistor in the negative side of the plate power supply. As the plate current varies with power, R55 is included for level adjustment. Positive five volts output can be obtained by varying R55. The output is clamped with a 15 volt zener diode for circuit protection.

1–65. U16B functions as a non–inverting amplifier with a gain of one. The input is obtained from the low–potential end of the plate meter multiplier circuit board. Positive five volts corresponds to full–scale plate voltage.

1–66. **POWER SUPPLY CIRCUIT BOARD.** AC power is input to the controller through a voltage range selector which additionally provides overload protection and RFI isolation for the ac input (see Figure 1–3). A special power transformer with a tapped dual primary allows operation from both 50 and 60 Hz and a wide range of ac voltages without component changes. The primary and secondary windings are electrostatically shielded from each other. The secondary windings of the transformer produce three ac potentials which are full–wave rectified and regulated into four dc sources which supply all operating voltages for the exciter circuitry. When power is applied to the controller, the cooling fan will run continuously.

1–67. **Positive Fifteen Volt Controller Supply.** A 20.4 volt secondary of transformer T1 is full–wave bridge–rectified into a +27.5 volt supply by diodes D1, D2, D7, and D8 and filtered by capacitor C1. This rectified voltage is routed to U1 which regulates the input potential to a +15 volt source for the controller logic circuitry. The output potential is adjusted by R3. Diode D19 prevents capacitor and battery discharge through the regulator biasing circuit during power failures.

1–68. Integrated circuit U1 is a three–terminal adjustable positive regulator containing internal thermal overload protection and short–circuit current limiting features. Further protection for U1 is provided by diode D16 which protects the regulator from a reverse polarity potential applied to the output.